IN THE CLAIMS

Please amend the claims as follows:

1. (Previously Presented) A system comprising:

a storage element;

a memory hierarchy coupled to the storage element;

a processor coupled to the memory hierarchy, wherein the processor is configured to test itself by repeatedly executing a plurality of instructions using a replay handler loaded into the memory hierarchy.

2. (Original) The system of claim 1 wherein the memory hierarchy is an instruction cache.

3. (Previously Presented) The system of claim 1 wherein the replay handler is loaded into the memory hierarchy in response to a signal.

4. (Previously Presented) The system of claim 1 wherein the replay handler includes the plurality of instructions.

5. (Previously Presented) The system of claim 1 wherein the replay handler loads the plurality of instructions into the memory hierarchy from an external device.

6. (Previously Presented) A system for replaying executions comprising:

a storage element;

a memory hierarchy coupled to the storage element;

a system bus coupled to the memory hierarchy; and

a processor coupled to the system bus, wherein the processor executes instructions from the memory hierarchy and wherein on a break, the processor reaches a steady state, transfers original code of the memory hierarchy to the storage element, loads a replay handler into the memory hierarchy and the processor executes the replay handler to repeatedly replay at least one

execution to test for proper operation of the processor, wherein the at least one execution includes a plurality of instructions.

7. (Previously Presented) The system of claim 6 wherein the original code is loaded into the memory hierarchy after the at least one execution has been repeatedly replayed.

8. (Original) The system of claim 6 further comprising a system memory and wherein the storage element is a location in the system memory.

9. (Original) The system of claim 6 wherein the storage element is a hard drive.

10. (Previously Presented) A system comprising:

a memory hierarchy;

a processor coupled to the memory hierarchy wherein the processor executes instructions from the memory hierarchy;

a port coupled to the processor and memory hierarchy;

a host system coupled to the port; and

wherein the host system generates a replay handler generates at least one execution to be repeatedly replayed by the processor when executing the replay handler, and generates a signal to the processor to cause the processor to load the replay handler into the memory hierarchy and repeatedly replay the at least one execution.

11. (Original) The system of claim 10 wherein on the signal, original code of the memory hierarchy is saved, the replay handler is loaded into the memory hierarchy from the host system through the port, and the replay handler is executed by the processor.

12. (Original) The system of claim 11 wherein on the replay handler being executed, the replay handler is modifiable by the host system.

13. (Original) The system of claim 12 wherein the replay handler is modified to alter starting and stopping points of one of the at least one executions.

14. (Original) The system of claim 10 wherein a replay state is sent to the host system through the port.

15. (Original) The system of claim 10, wherein the port is a network interface.

16. (Original) The system of claim 10, wherein the port is a serial interface.

17. (Currently Amended) A method for replaying executions comprising:

interrupting normal processor execution;

loading a replay/restart kernel into a memory hierarchy;

repeatedly replaying at least one execution to test for proper operation of a processor, wherein the at least one execution includes a plurality of processor instructions; and

resuming normal executions.

18. (Original) The method of claim 17 further comprising generating the at least one execution.

19. (Original) The method of claim 18 further comprising accessing state information.

20. (Previously Presented) A method comprising:

interrupting processes executing on a processor;

storing minimal state information sufficient to later resume the interrupted processes;

storing original code of an instruction cache;

loading a replay handler into the instruction cache;

branching execution of the processor to the replay handler;

replaying a system execution a number of times from a starting point to a stopping point while monitoring state information to test for proper operation of the processor;

loading the original code into the instruction cache; and

resuming interrupted processes utilizing the minimal state information.

21. (Original) The method of claim 20 further comprising:

modifying the number of times, the starting point and the stopping point by a user.

22. (Original) The method of claim 20 further comprising:

generating the system execution by tracing an execution of a program.

23. (Currently Amended) A computer readable medium containing computer instructions for instructing a processor to perform a method of:

generating at least one execution that includes a plurality of processor instructions;

interrupting normal processing;

loading a replay handler into a memory hierarchy;

repeatedly replaying the at least one execution to test for proper operation of the processor;

accessing state information;

storing state information; and

resuming normal processing.